



Data Recovery VLIUUB

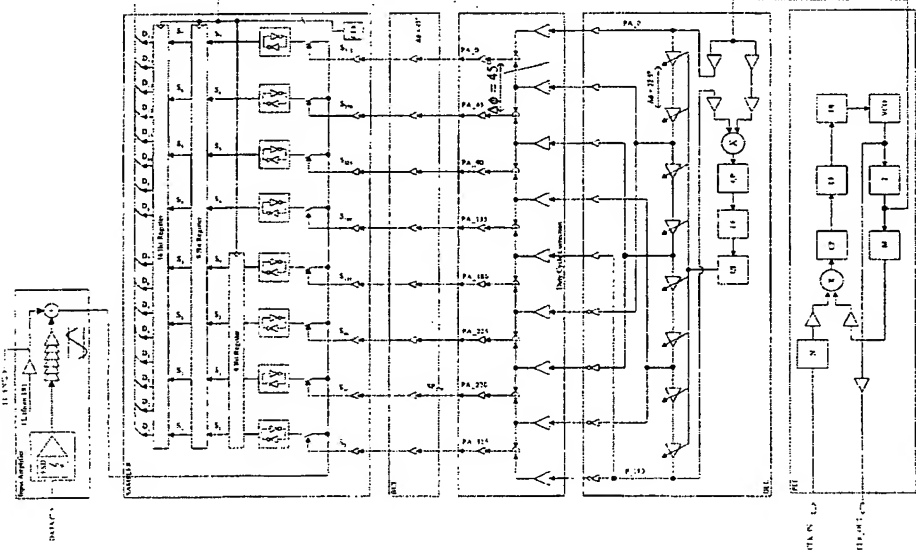
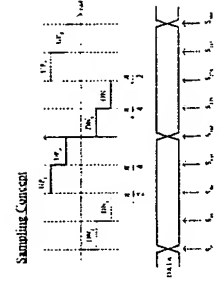
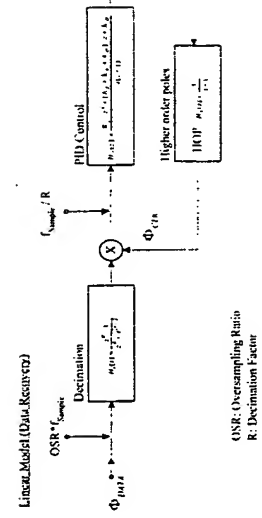


Fig. 1



IIUB Receiver Section
COMUSCE Patents
Version 1.0 (May 2004)

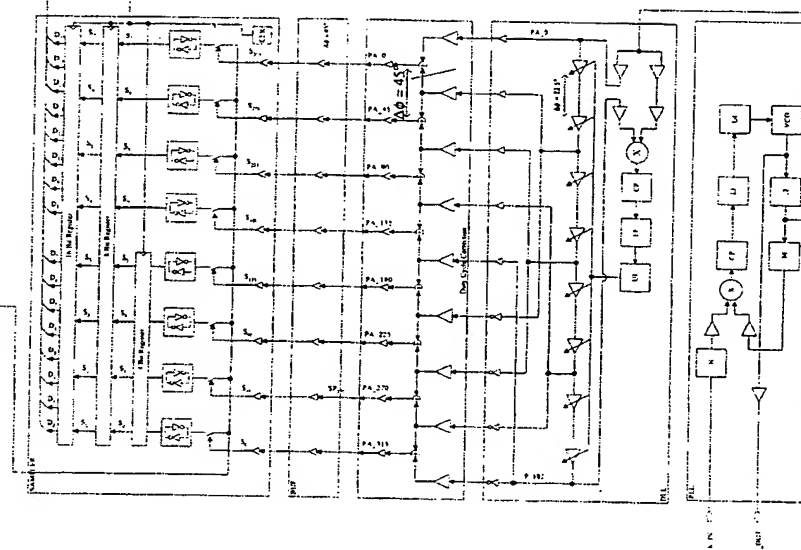
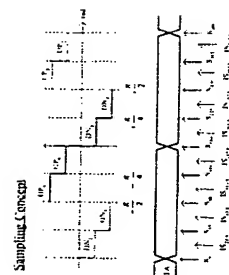
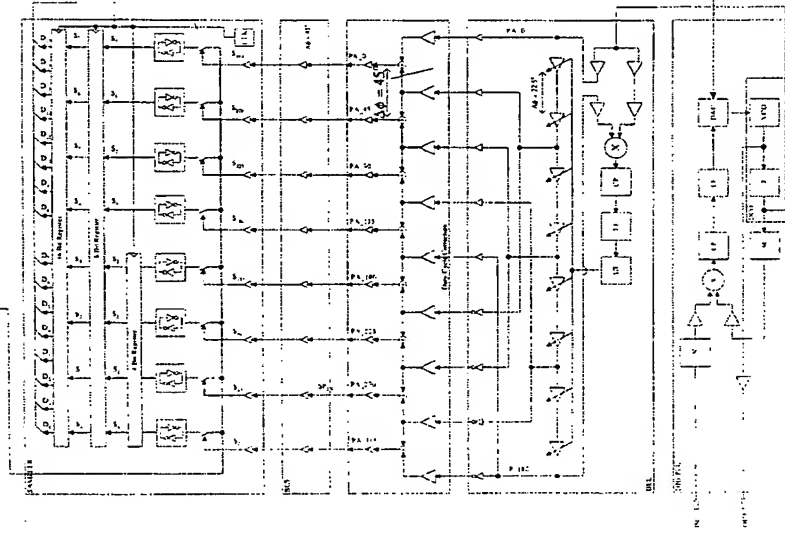
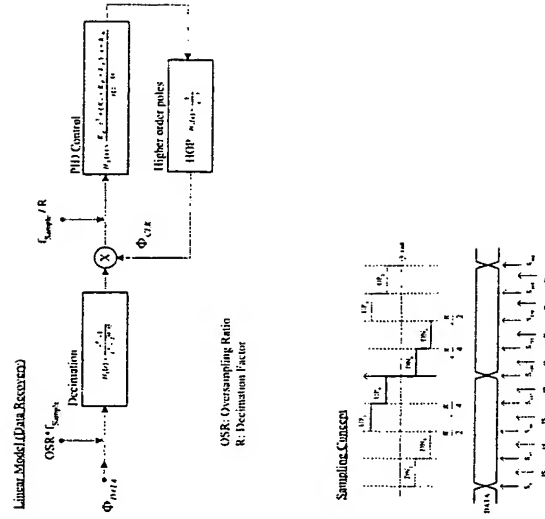
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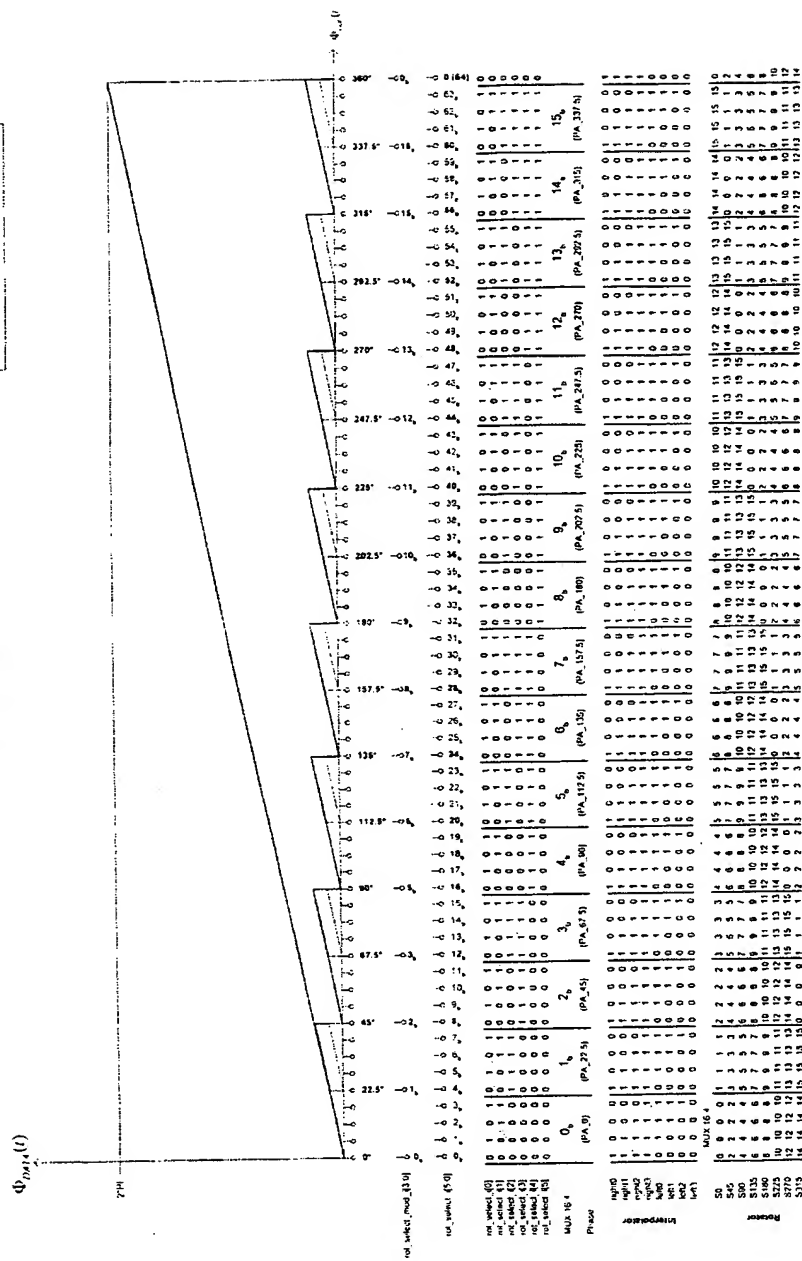
Figure 1 is a block diagram of the data reduction system. It shows the flow of data from the input transducer through acquisition, processing, and display to a final decoder. Key components include the Data Acquisition block with a Data Buffer and Data Processor, the Display block showing a waveform, and the Decoder block. Power is supplied by a Battery and a Power Supply.



[illegible][illegible]

HUB Receiver Section
COM ONCE P. Gregorius
Version 1.0 / 06.03.2003

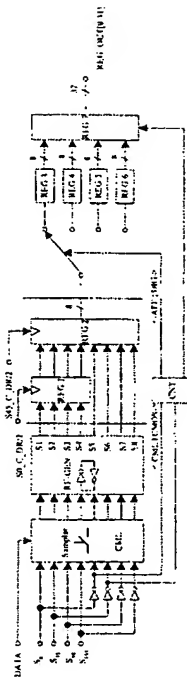
Fig. 4



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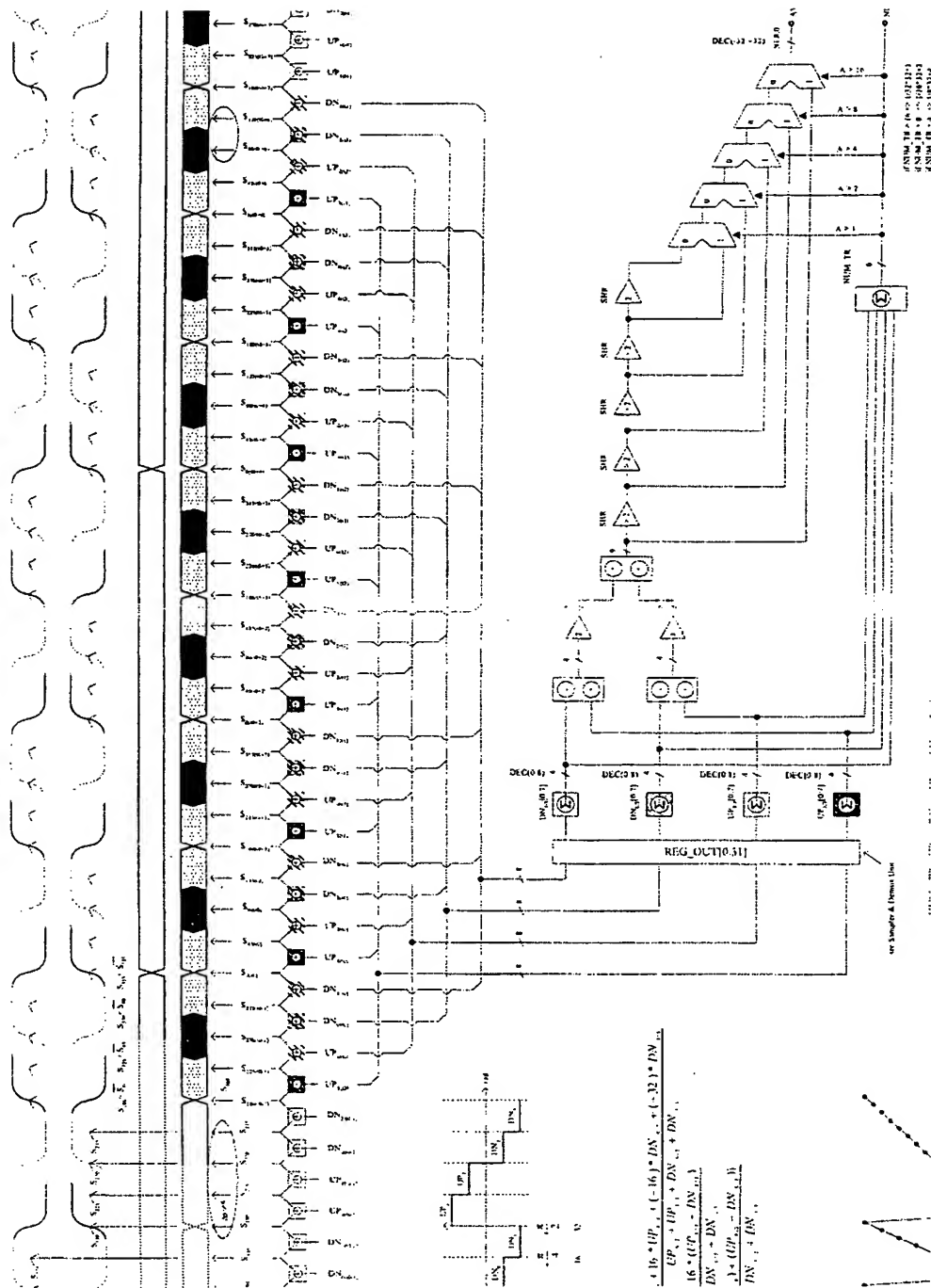
Timing diagram



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Version 0.1

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Half Rate Phase Detection Algorithm (Timing Recovery)



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